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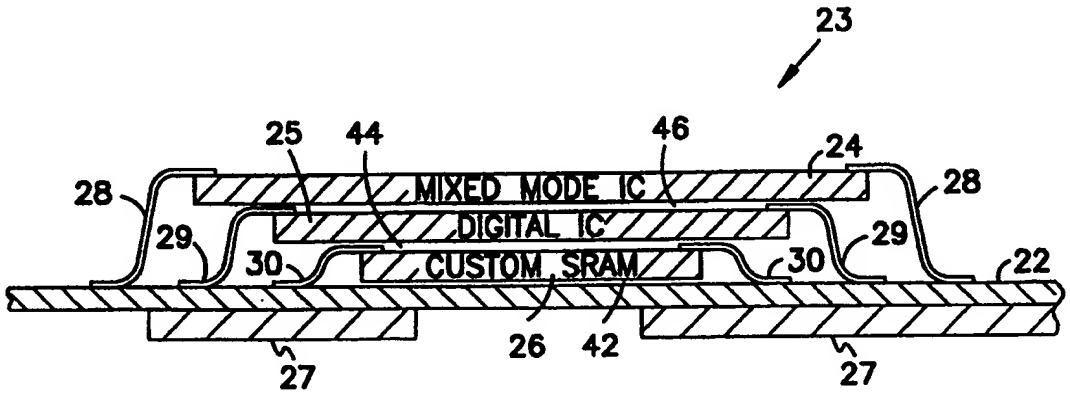

(57) Abstract

A stacked integrated circuit assembly for an implantable medical device. The circuit assembly is carried on a printed circuit board substrate and has a first integrated circuit die disposed on the substrate. The first die has a plurality of leads extending outwardly therefrom which are electrically bonded to the substrate. A second die is larger than and stacked vertically over the first die. The second die has a plurality of leads extending outwardly therefrom which are bonded to the substrate. The first die is bounded within the leads of the second die and sandwiched between the second die and the substrate. Additional dies may be stacked in a similar manner as desired for a particular application.

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STACKED INTEGRATED CIRCUITS USING TAPE AUTOMATED BONDING WITHIN AN IMPLANTABLE MEDICAL DEVICE

Field of the Invention

The present invention relates to implantable medical devices and, more particularly, this invention relates to a device utilizing stacked integrated circuits for producing a smaller implantable device and to a method of making the same.

Background of the Invention

Pulse generators in the form of a pacemaker or defibrillator implanted in the body for electrical cardioversion or pacing of the heart are well known. More specifically, electrodes implanted in or about the heart have been used to reverse (i.e., defibrillate or cardiovert) certain life threatening arrhythmias, or to stimulate contraction (pacing) of the heart, where electrical energy is applied to the heart via the electrodes to return the heart to normal rhythm. Electrodes have also been used to sense near the sinal node in the atrium of the heart and to deliver pacing pulses to the atrium. The electrode in the atrium positioned near the sinus node of the heart senses the electrical signals that trigger the heartbeat. The electrode detects abnormally slow (bradycardia) or abnormally fast (tachycardia) heartbeats. In response to the sensed bradycardia or tachycardia condition, a pacemaker or pulse generator produces corrective pulses or signals and delivers them via the electrodes to alleviate the condition.

The sick sinus syndrome and symptomatic AV block constitute the major reasons for insertion of cardiac pacemakers today. Cardiac pacing may be performed by the transvenous method or by electrodes implanted directly onto the ventricular epicardium. Transvenous pacing may be temporary or permanent. In temporary transvenous pacing, an electrode lead is introduced into a peripheral vein and fluoroscopically positioned against the endocardium of the right atrium or right ventricle. The proximal electrodes are connected to an external cardiac pacemaker which has an adjustable rate and milliamperage

control. Temporary transvenous pacing is utilized (1) prior to the insertion of a permanent pacing system and (2) in situations in which the indication for pacing is judged to be reversible (drug-induced AV block or bradycardia) or possibly irreversible and progressive (AV and bundle branch blocks associated with myocardial infarction). Permanent transvenous pacing is performed under sterile surgical conditions. An electrode lead is generally positioned in the right ventricle or in the right atrium through a subclavian vein, and the proximal electrode terminals are attached to a pulse generator which is implanted subcutaneously. Another sense electrode may be positioned within the atrium of the heart near the sinus node.

A permanent pulse generator is implanted during a surgical procedure under the skin of an individual. One desirable characteristic of such a device is that it have a relatively small volume or size. This is to increase the comfort, to prevent protrusion of the device from beneath the skin, and to prevent interference of the device with adjacent vital organs of the individual. One way to reduce the size of the implants is to utilize small electronic components within the device. The overall size of the implant is determined by the size, orientation and quantity of the various components.

The primary electronic component of an implantable medical device is the printed circuit board. The board typically includes thereon a number of integrated circuits which provide the logic, static memory and other electronic features of the device. The board typically also includes interconnects for electrically linking the circuits and other components such as capacitors, resistors, diodes, transistors, transformers, and reed switches. One problem with conventional implantable devices having two or three integrated circuits is that the board must have a large enough surface area to support each of the circuits disposed side by side and support the other components as well.

Another problem with conventional implantable devices is that the interconnects must run between the side by side circuits and between the circuits and other components. The length of the interconnects can be quite long in a typical construction. The longer the electronic path between components,

the slower the electronic response for that path and the more difficult it becomes to route the interconnects within the confines of the board.

In the field of computers, dynamic random access memory or DRAM integrated circuit dies have been stacked one on top of the other on printed circuit boards to save space. Such a die stack for a computer printed circuit board has utilized only DRAM circuits of identical size within a particular stack and has not utilized application specific integrated circuits (ASIC's).

One attempted solution to the above problems specifically related to the use of ASIC's within medical devices is to stack the dies with the largest being placed on and epoxied to the board substrate and the additional circuits stacked and epoxied thereon from largest to smallest and being epoxied to one another. This construction has been incorporated into circuit assemblies provided by Sulzer Intermedics, Inc. of Angleton, Texas which utilized conventional wirebonding to connect the dies to the board interconnect pads. The dies were also tested and burned-in only in wafer form. Any later occurring flaws or malfunctions in a die would not be detected until the dies have already been attached to the board.

One problem with the above solution is that by stacking from largest to smallest, the wirebond leads are exposed and must be protected from damage during further manufacturing steps. The wirebond leads also add to the height of the stack which is undesirable when the goal is to reduce the overall size of the device. Another problem with this attempted solution is that the devices must be reworked or scrapped if one or more of the dies turns out to be a malfunctioning unit.

There is a real need for an implantable medical device which utilizes stacked ASIC's for size reduction of the devices. A pacemaker or defibrillator equipped with a stacked ASIC assembly would produce a smaller implantable device. In addition, there is a need for an implantable medical device which utilizes only known good dies for the ASIC's preventing the added labor and expense of either scrapping or reworking devices once the boards have been assembled. There is also a need for an implantable medical device which

simplifies and shortens the interconnect routing between the various electronic components of the device.

Summary of the Invention

A medical device such as a pulse generator adapted for implantation about the heart and for monitoring or stimulating cardiac activity includes a stacked integrated circuit assembly on the printed circuit board. The integrated circuit assembly includes a first integrated circuit die disposed on the substrate. The first die has a perimeter edge with a plurality of leads extending outwardly therefrom which are electrically bonded to the substrate defining a first footprint thereon.

A second integrated circuit die is larger than and stacked vertically over the first die. The second die also has a plurality of leads extending outwardly from its perimeter. These leads are also bonded to the substrate and define a second footprint thereon. The first footprint is smaller than and bounded by the second footprint such that the first die and its leads are sandwiched between the substrate and the second die. In other embodiments, the circuit assembly may include additional dies stacked similar to and over the first two dies, limited only by the height restrictions for a given application.

The invention also contemplates a method of fabricating a substrate for an implantable medical device which incorporates the above stacked circuit assembly. The method includes selecting several known good dies from a plurality of integrated circuit dies and selecting and providing a suitable substrate having a plurality of lead pads thereon. The lead pads must correspond to the leads of the dies to be bonded to the substrate.

The method also includes utilizing the tape automated bonding process to electrically bond the leads of each die to its corresponding lead pads on the substrate. The dies are again placed in a vertical stack having successively larger dies stacked over smaller ones. The dies may be spaced apart from one another defining gaps between them or may be epoxied to their adjacent dies or the substrate using an epoxy to increase mechanical stability. Alternatively, a thermally conductive epoxy may be used.

Brief Description of the Drawings

FIG. 1 is a perspective view of a printed circuit board including a stacked integrated circuit assembly of the invention for an implantable pulse generator.

FIG. 2 is a top plan view of the printed circuit board of FIG. 1 where the stacked integrated circuit assembly has been removed from the substrate.

FIG. 3 is a cross sectional view of the stacked integrated circuit assembly of FIG. 1.

FIG. 4 is a cross sectional view of another embodiment of the stacked integrated circuit assembly.

Description of the Preferred Embodiment

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which are shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Referring now to the drawings, Figure 1 is a perspective view of a relatively small printed circuit board 20 for inclusion in an implantable medical device such as a pacemaker or a defibrillator (not shown). The board 20 of the invention includes a substrate 22 for carrying thereon a number of electronic components such as a stacked integrated circuit assembly 23. As shown in Figure 3, circuit assembly 23 includes three stacked application specific integrated circuit (ASIC) dies 24, 25, and 26, and other components 27. Each of dies 24, 25 and 26 further includes a plurality of tape automated bonded (TAB) leads 28, 29 and 30 connecting the dies to the substrate to interconnect them with one another and with the other components on the board.

TAB integrated circuits have leads which extend from at least two sides of the die package. The leads are bonded to corresponding interconnect pads 32, 33 and 34 on the circuit board via any number of conventional methods discussed below. TAB leads have a thin profile and are placed closely together

on the die package permitting a relatively high density interconnect system as compared to other types of interconnect systems. Because the leads are thin, they produce a lower profile connection between the die package and the board than conventional pin-through or pin-grid array type connections or wire bonded connections. An ASIC is an integrated circuit design which performs a repetitive predetermined function. The TAB of the ASIC permits burning-in of the desired circuit patterns or paths after the die has been separated from a wafer and allows for known good die testing at essentially the same time or after burn-in.

A typical ASIC is first back ground in the wafer form to achieve the thinnest possible die profile and then cut or separated from the wafer. The ASIC is then inner lead bonded to attach the leads extending outward from the perimeter edge of the die package. Then the dies are given a protective coating, tested and finally the desired circuit function is burned-in. One aspect of the present invention involves selecting known good ASIC dies and stacking two or more selected dies, one on top of the other, on the board substrate 22. As illustrated in Figures 3 and 4, the stack is created by first mounting the smallest known good die 26 adjacent the substrate 22 and bonding the leads 30 to the board by hot bar solder reflow. The additional dies are then stacked over the smallest die from smallest to largest (die 25 to 24 in this example) and bonded to the board in a similar manner. Thus, the die footprint on substrate 22 is only as large as the largest die 24, which is best illustrated in Figures 1 and 2.

One advantage of this inverted stack is that the leads 28, 29 and 30 of the dies 24, 25 and 26 are disposed very close to one another. This is best illustrated in Figure 2 showing the interconnect lead pads 32, 33, 34 for connecting leads 28, 29 and 30, respectively, to the board. The lead pads 32 define a footprint 38 on the substrate for the largest die 24. Similarly, the lead pads 33 define a footprint 37 for die 25 and lead pads 34 define a footprint 36 for the smallest die 26. The footprint 36 for the smallest die is bound within the footprint 37 for the middle die. The footprint 37 is bound within the footprint 38 for the largest die 24. This arrangement substantially shortens the distance of

and simplifies the routing of interconnects between the various dies and other components of the board.

The potential to stack additional ASIC dies exists and is essentially only limited by the total permissible stack height for a given application. Although the die shown in Figures 3 and 4 are stacked face-up, the die can be face down and are considered within the scope of the present invention. Face down die provide advantages in some situations where 2 die have a similar size. The face down die would permit a smaller foot print for the die closest to the substrate.

Other means for connecting the leads to the interconnect pads may also be used including gold to gold bonding, individual lead soldering, or conductive adhesive attachment. In the embodiment of Figure 3, the ASIC's are spaced from one another permitting air to flow through the stack between the dies. A gap 42 is defined between die 24 and 25, a gap 44 is defined between die 26 and 25, and a gap 46 is defined between die 26 and substrate 22. Waste heat is at least partly dissipated by being transferred to the air as it passes through the gaps and is subsequently transferred to the case of the device (not shown).

Figure 4 illustrates another embodiment of the three die stack assembly 23 wherein the dies are epoxied directly to one another. An epoxy 50 is disposed between the die to fill gaps 42, 44 and 46 and is applied to attach each die to an adjacent die or the substrate as the stack is created. In one embodiment, a thermally conductive epoxy. If no such epoxy is used, the strength of the leads 28, 29 and 30 must be relied upon to support the mass of each die 24, 25 and 26, respectively. Since the leads are TAB type bonded, they are relatively thin. The longer the lead, the more susceptible the lead will be to collapsing under the weight of its respective die. Hence, use of epoxy 50 between the dies is desirable for stack assemblies 23 having more than several die in order to stabilize and to support the dies above the substrate. In addition, the epoxy adds rigidity to the stack assemblies 23, which aids in preventing handling damage in subsequent manufacturing steps.

The process involved in preparing a die for fabricating a medical device according to the invention involves several steps. First, a wafer is tested to determine which of the dies have electrically functioning circuitry. Next, the wafer is back ground to achieve a thin die profile. For example, a current medical device manufactured by the assignee of the present invention requires a die profile of 0.019 inches. Additionally, tests have demonstrated that die having a profile of 0.008 inches can be produced and utilized in the stacked assembly of the invention. The next step includes sawing the wafer into individual dies and selecting the functional dies. The next steps involve inner lead bonding the dies to the perimeter leadframe, adding a protective coating to the circuit area of the dies, and then testing to determine which are known good dies. The final step prior to assembly of the dies to the board is to burn-in the desired circuit for a particular application and selecting the known good die from the lot.

The known good die are then mounted to a substrate populated with various electronic components to produce the substrate assembly. These steps include first, dispensing flux onto the outer lead bond or interconnect pads 32, 33 and 34 of the substrate 22. Next, the bottom or smallest good die 26 is loaded into a TAB bonder. The TAB bonder excises and leadforms the die 26, inspects the leads 30, aligns the die to its respective pads 34 on the substrate 22, and bonds the die to the substrate by a hot bar solder reflow or other suitable technique. Alternatively, the die is bonded to the substrate using gold to gold bonding, thermal compression, or conductive adhesive such as thermal plastic or silver epoxy.

These steps are then repeated for each of the remaining die 25 and 24 of the stack. The completed substrate assembly 20 is then cleaned to remove any excess flux residue. The additional step of adding the epoxy 50 between the dies 24, 25 and 26 of the assembly 23 may be included to provide supplemental mechanical stability to the device as described above. The epoxy 50 is added to the substrate to mate with the smallest die 26. Epoxy 50 is also added to the die 26 to mate with middle die 26 and to the larger die 24 to mate with die 25. A

suitable epoxy which has been tested and found effective for the invention is of a quick curing type. The epoxy utilized cured in less than 5 minutes at about 150°C.

The invention provides several important advantages. By stacking dies on the substrate instead of placing the dies adjacent one another, significant space savings is accomplished in the X-Y plane or surface area of the substrate. This is because space is needed on the substrate only for the footprint of the largest die and not for all three dies. Additionally, space savings in height or the vertical Z axis of the board is achieved by utilizing TAB leadforms, which are lower in profile than wirebonded leads. Also, only known good die, tested after the final process step in producing the dies, are committed to the substrate. This greatly reduces the need to either scrap printed circuit boards having non-functioning dies or to rework a board to replace a non-functioning die. Further, the invention reduces the length and simplifies the routing for the interconnects between the dies and also between the dies and other components on the substrate. This is accomplished by having all the leads of the dies contact the board in very close proximity to one another as illustrated in Figure 2, reducing the line lengths between pads. Additionally, the substrate assembly provides a sturdy construction for subsequent manufacturing steps, avoiding harm to the leads and the dies within the stack. The formed leads are lower in profile than wirebonds, therefore being susceptible to damage during further manufacturing steps. Without wirebonded leads, it is not necessary to utilize expensive and intricate tooling to protect the wirebonds during subsequent manufacturing steps. An epoxied assembly further adds to the stability and the sturdiness of the device.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A substrate assembly comprising:

a substrate;

a first integrated circuit disposed on said substrate, said first integrated circuit having a first perimeter edge with a plurality of first leads extending outwardly from at least a portion of the first perimeter edge and being electrically bonded to said substrate and defining a first footprint thereon;

a second integrated circuit which is larger than and stacked vertically over said first integrated circuit, said second integrated circuit having a second perimeter edge with a plurality of second leads extending outwardly from at least a portion of the second perimeter edge and being bonded to said substrate and defining a second footprint thereon; and

said first footprint being smaller than and at least partially bounded by said second footprint.

2. The substrate assembly of claim 1, wherein said first leads and said first integrated circuit are captured between said substrate and said second integrated circuit.

3. The substrate assembly of claims 1 or 2, wherein said first and second integrated circuits are application specific integrated circuit known good dies.

4. The substrate assembly of claims 1, 2, or 3, further comprising a third integrated circuit which is larger than and stacked vertically over said second integrated circuit, said third integrated circuit having a third perimeter edge with a plurality of third leads extending outwardly therefrom and being bonded to said substrate and defining a third footprint thereon, said second footprint being smaller than and at least partially bounded by said third footprint.

5. The substrate assembly of claim 4, wherein said second leads and said second integrated circuit are captured between said first and said third integrated circuits.

6. The substrate assembly of claim 4, wherein said first, second and third integrated circuits are application specific integrated circuit known good dies.

7. The substrate assembly of claims 1, 2, 3, 4, 5, or 6, wherein said first leads are electrically bonded to said substrate by the process of tape automated bonding.

8. The substrate assembly of claims 1, 2, 3, 4, 5, 6, or 7, wherein said second leads are electrically bonded to said substrate by the process of tape automated bonding.

9. The substrate assembly of claim 4, wherein said third leads are electrically bonded to said substrate by the process of tape automated bonding.

10. The substrate assembly of claims 1, 2, 3, 4, 5, 6, 7, 8, or 9, wherein said first integrated circuit is spaced from said substrate defining a first gap therebetween.

11. The substrate assembly of claim 10, further comprising epoxy disposed within said first gap for attaching said first integrated circuit to said substrate.

12. The substrate assembly of claims 1 or 10, wherein said second integrated circuit is spaced from said first integrated circuit defining a second gap therebetween.

13. The substrate assembly of claims 11 or 12, further comprising epoxy disposed within said second gap for attaching said second integrated circuit to said first integrated circuit.

14. The substrate assembly of claim 4, wherein said third integrated circuit is spaced from said second integrated circuit defining a third gap therebetween.

15. The substrate assembly of claim 14, further comprising epoxy disposed within said third gap for attaching said third integrated circuit to said second integrated circuit.

16. The substrate assembly of claim 1, further comprising a third integrated circuit stacked vertically over said second integrated circuit, said third integrated circuit having a third set of side edges with a plurality of third leads extending outwardly from at least two of the third side edges, the third leads being bonded to said substrate and defining a third footprint thereon; and

said second footprint being smaller than and at least partially bounded by said third footprint

17. The substrate assembly of claim 16, wherein said second leads and said second integrated circuit are captured between said substrate and said third integrated circuit.

18. The implantable medical device of claims 16 or 17, further comprising thermally conductive epoxy disposed between the first and second integrated circuits.

19. A method of fabricating a substrate assembly for an implantable medical device, said method comprising:

electrically bonding a plurality of first leads extending from a perimeter edge of a first known good die to a plurality of first lead pads on a substrate;

placing a second known good die having a plurality of second leads extending from a perimeter edge of the second known good die vertically over said first known good die; and

electrically bonding said plurality of second leads to a plurality of second lead pads surrounding the first lead pads on the substrate by the process of tape automated bonding such that said first known good die is captured between said second known good die and said substrate.

20. The method of claim 19, wherein the step of electrically bonding the plurality of first leads to the plurality of first lead pads comprises the step of electrically bonding the first leads to the first lead pads by the process of tape automated bonding.

21. The method of claims 19 or 20, further comprising the steps of:

placing a third known good die having a plurality of third leads extending from a perimeter edge of the third known good die vertically over said second known good die; and

electrically bonding said plurality of third leads to a plurality of third lead pads surrounding the second lead pads on said substrate by the process of tape automated bonding such that said second known good die is captured between said third known good die and said first known good die.

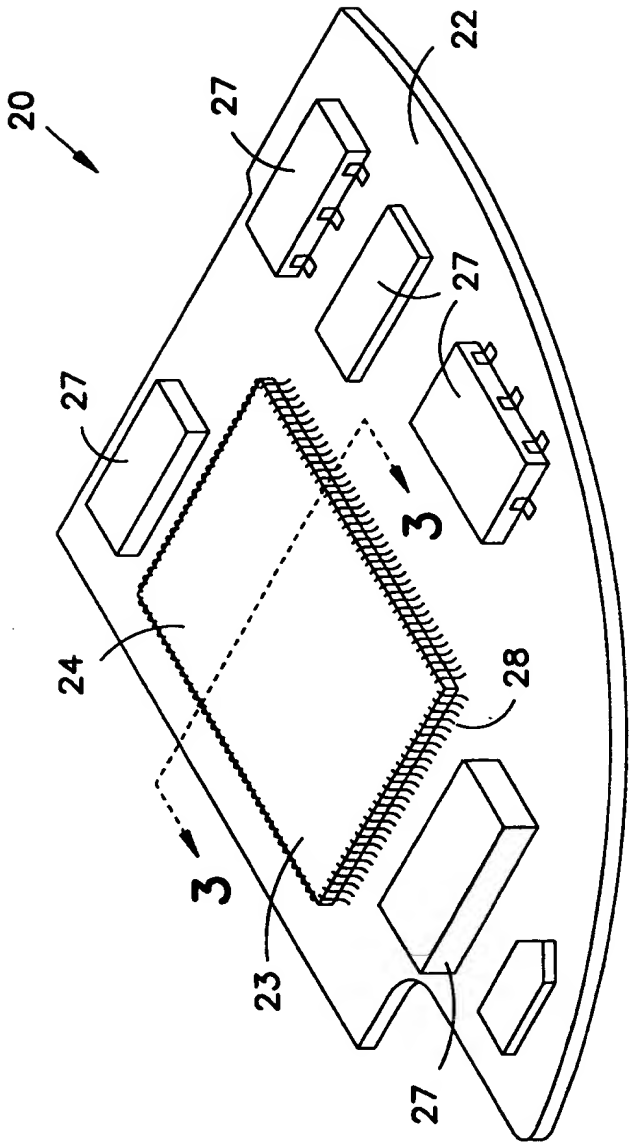


FIG. 1

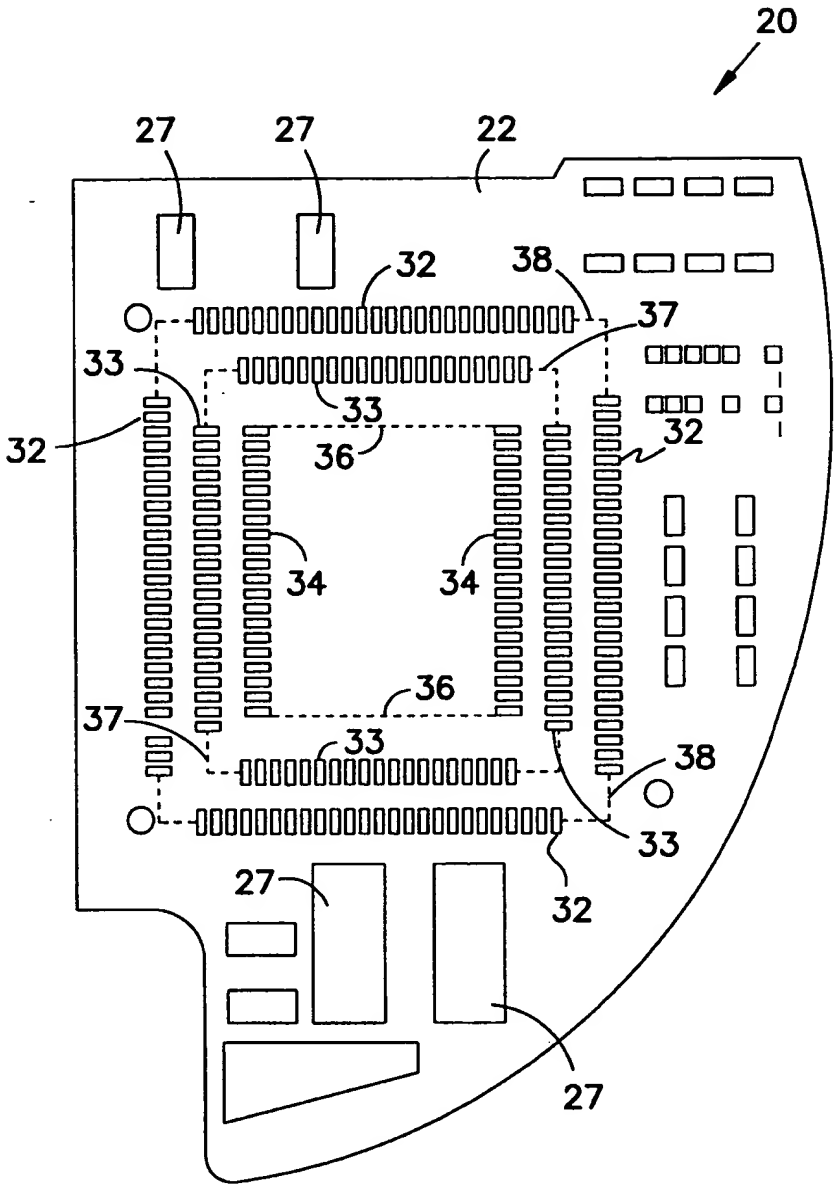
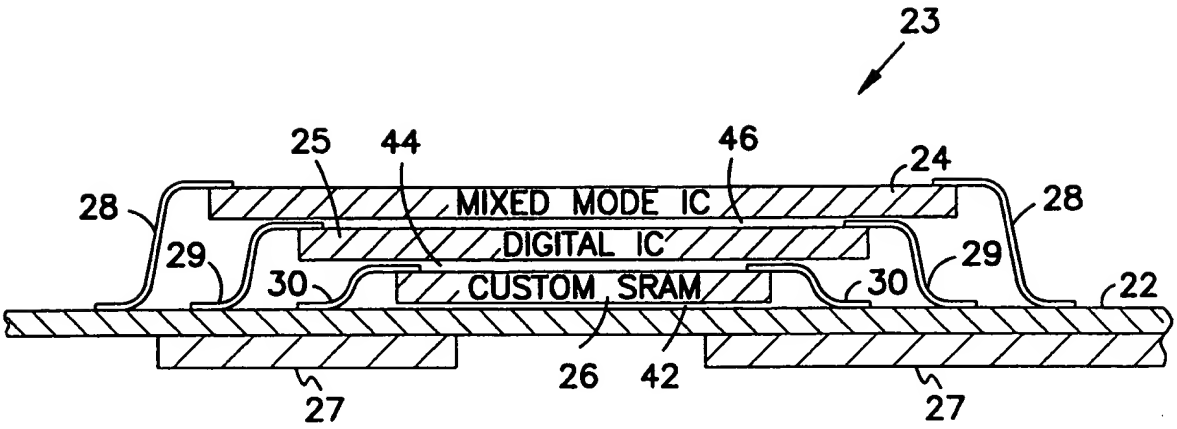


FIG. 2


23
25
44
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28
MIXED MODE IC
28
29
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42
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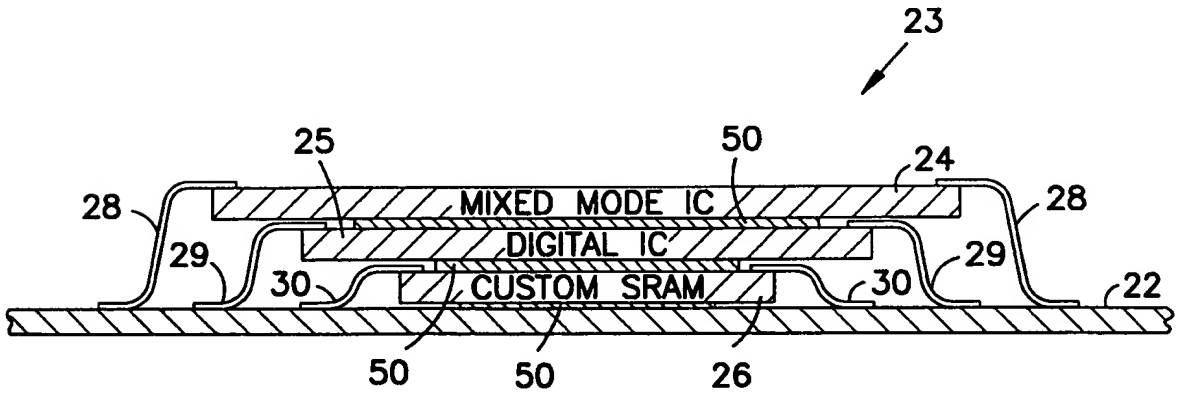
FIG. 3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MIXED MODE IC
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CUSTOM SRAM
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FIG. 4

INTERNATIONAL SEARCH REPORT

national Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L25/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

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IPC 6 H01L

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 008 (E-1486), 7 January 1994 & JP 05 251633 A (SONY CORP), 28 September 1993 see abstract	1,2,10, 12
A		3-9,11, 13-17

X	PATENT ABSTRACTS OF JAPAN vol. 012, no. 135 (E-604), 23 April 1988 & JP 62 261166 A (MATSUSHITA ELECTRONICS CORP), 13 November 1987	1,2,10, 12
A	see abstract	3-9,11, 13-17

A	US 5 587 341 A (MASAYUKI WATANABE ET AL) 24 December 1996 see column 1, line 29-31	1-18

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[X] Further documents are listed in the continuation of box C.

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INTERNATIONAL SEARCH REPORT

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PCT/US 98/21081

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 255 (E-1214), 10 June 1992 & JP 04 056262 A (MATSUSHITA ELECTRON CORP), 24 February 1992 see abstract	10-15
A	US 5 144 946 A (WEINBERG ALVIN H ET AL) 8 September 1992 see column 1	19-21

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

national Application No
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